FIG.1
CONVENTIONAL ART

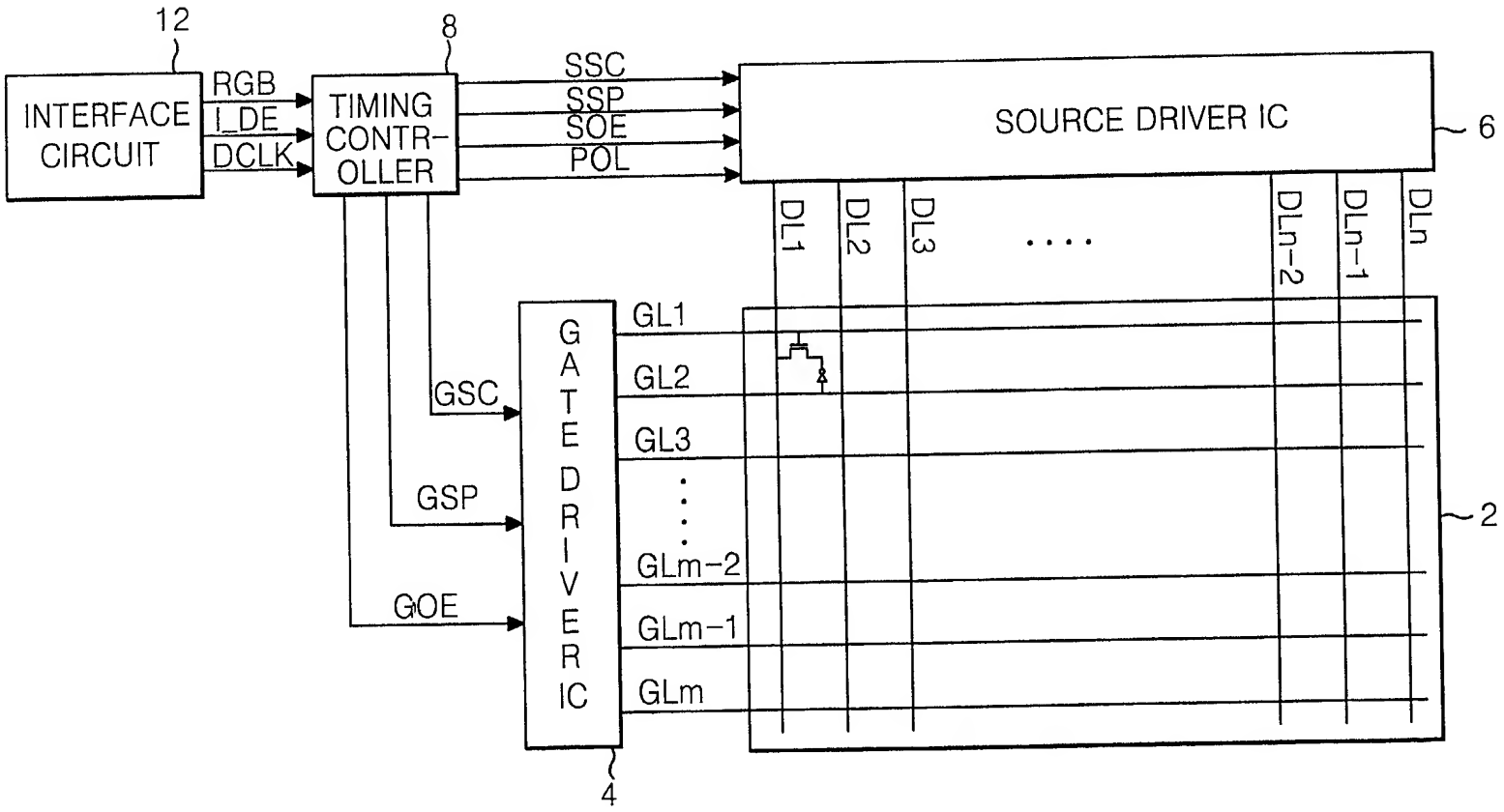


FIG.2
CONVENTIONAL ART

Video Mode	N	PinName
WHEN THE NUMBER OF DCLK AT DE BLANKING INTERVAL IS EVEN NUMBER(n)	1	Dclx [XGA 65MHz] (Falling Egde 에서 Latch)
	2	Video Data
	3	Data Lactch
	4	Toggle at Dclk Rising
	5	Odd Data La1ch
	6	FOUR TIMES Toggle SIGNAL INVERSION
	7	Even Data Latch
	8	FOUR TIMES Toggle SIGNAL INVERSION
	9	Even Data Latch
	10	FOUR TIMES Toggle SIGNAL INVERSION
	11	Even Data {D-IC INPUT Video Signal}
	12	Odd Data {D-IC INPUT Video Signal}
	13	Odd Enable
	14	SSP
WHEN THE NUMBER OF DCLK AT DE BLANKING INTERVAL IS ODD NUMBER(n+1)	15	FOUR TIMES Toggle SIGNAL INVERSION
	16	Even Data {D-IC INPUT Video Signal}
	17	Odd Data {D-IC INPUT Video Signal}
	18	Data Enable
	19	SSP

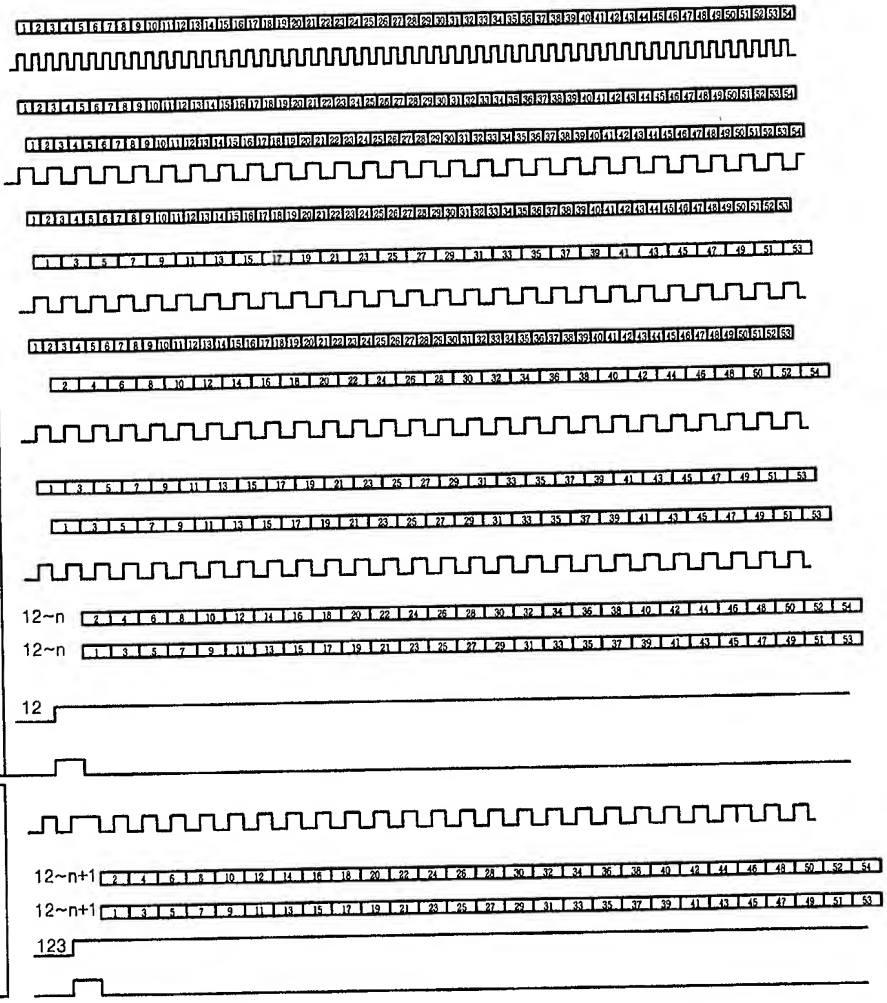


FIG.3
CONVENTIONAL ART

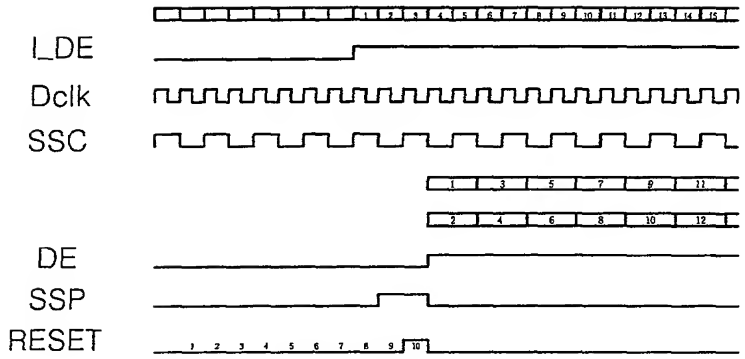


FIG.4
CONVENTIONAL ART

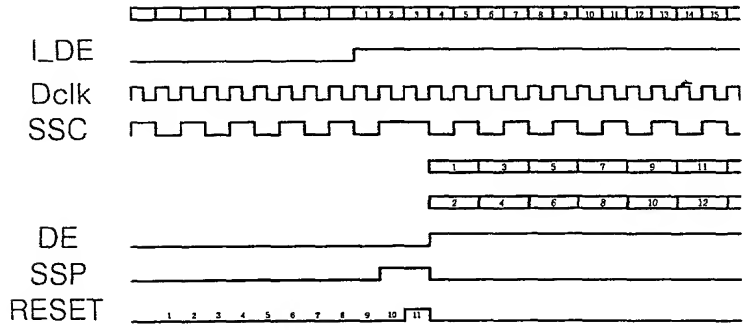


FIG.5

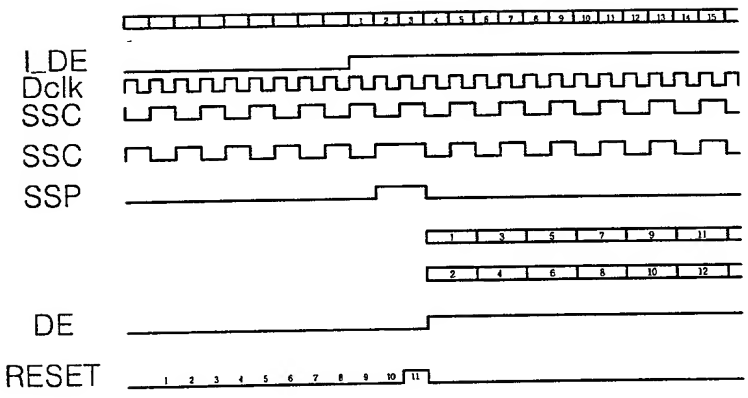
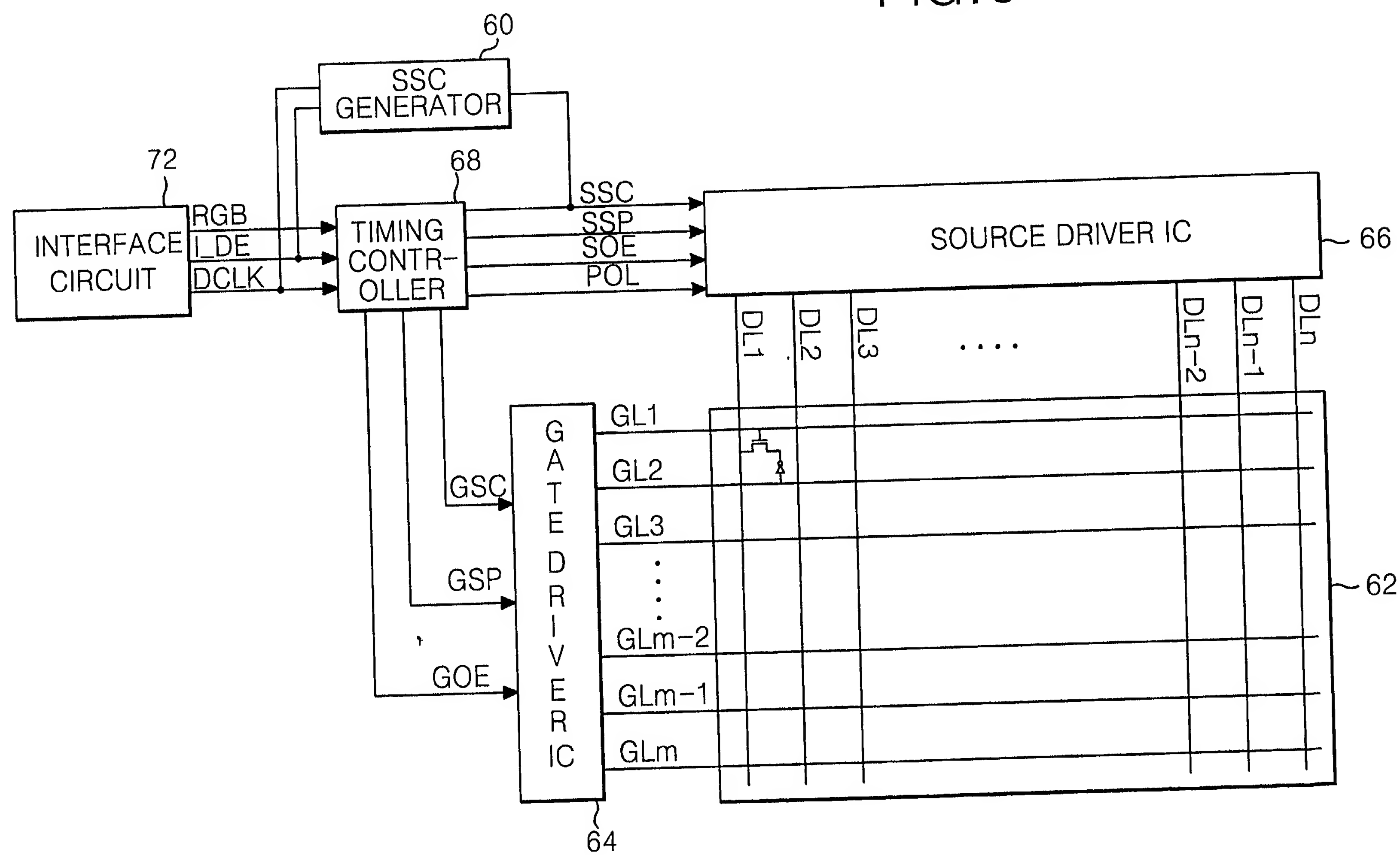


FIG.6



60
SSC GENERATOR
72
INTERFACE CIRCUIT
RGB
I_DE
DCLK
68
TIMING CONTR-OLLER
SSC
SSP
SOE
POL
SOURCE DRIVER IC
66
DL1
DL2
DL3
DLn-2
DLn-1
DLn
GSC
GSP
GOE
GATE DRIVER IC
64
GL1
GL2
GL3
GLm-2
GLm-1
GLm
62

FIG.7

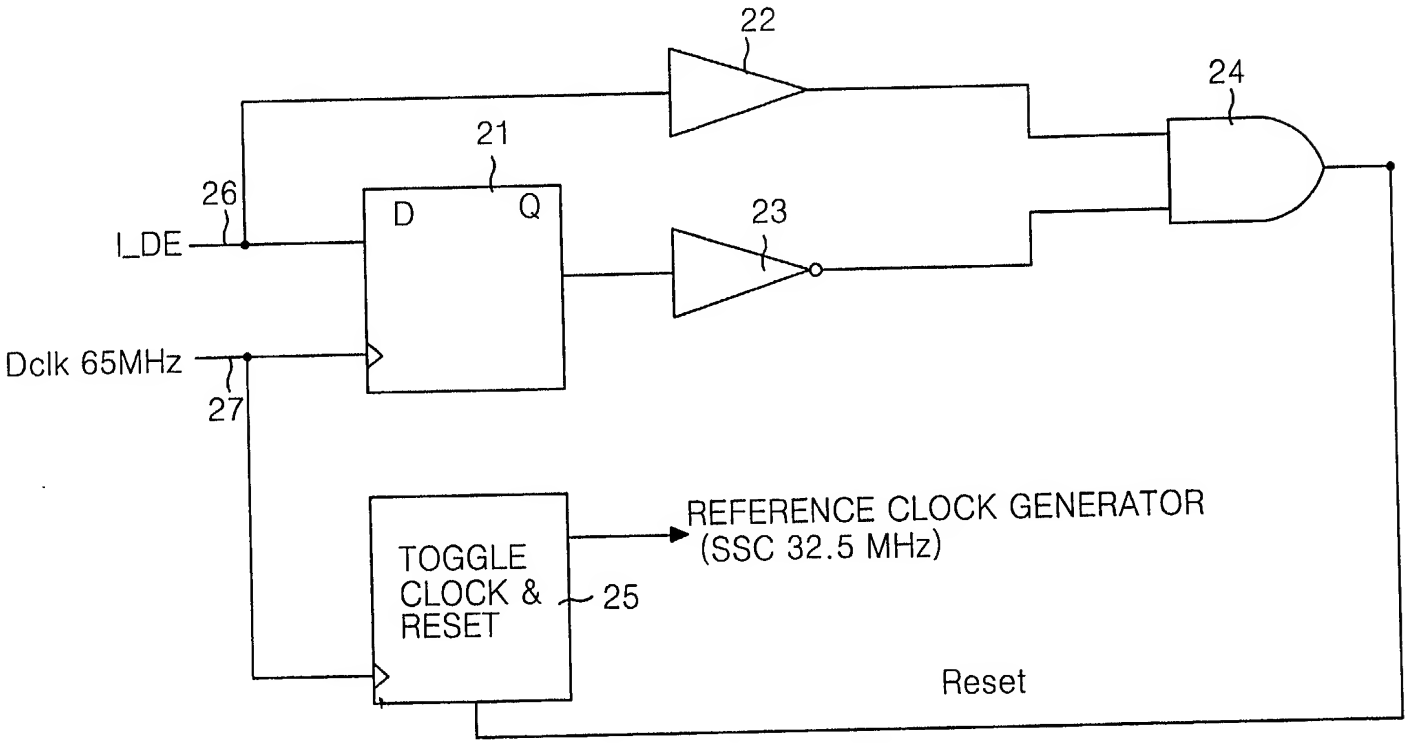


FIG.8

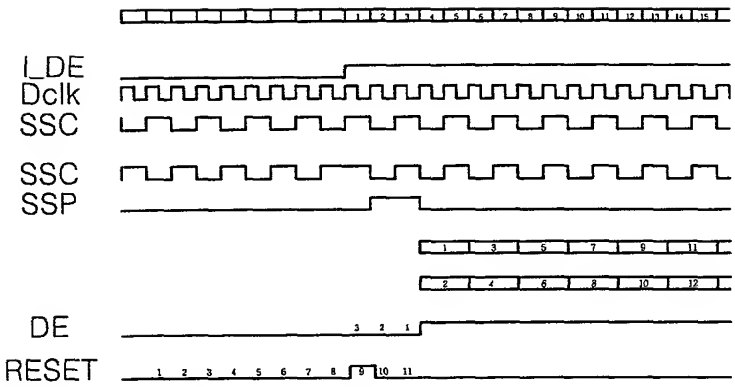


FIG.9A

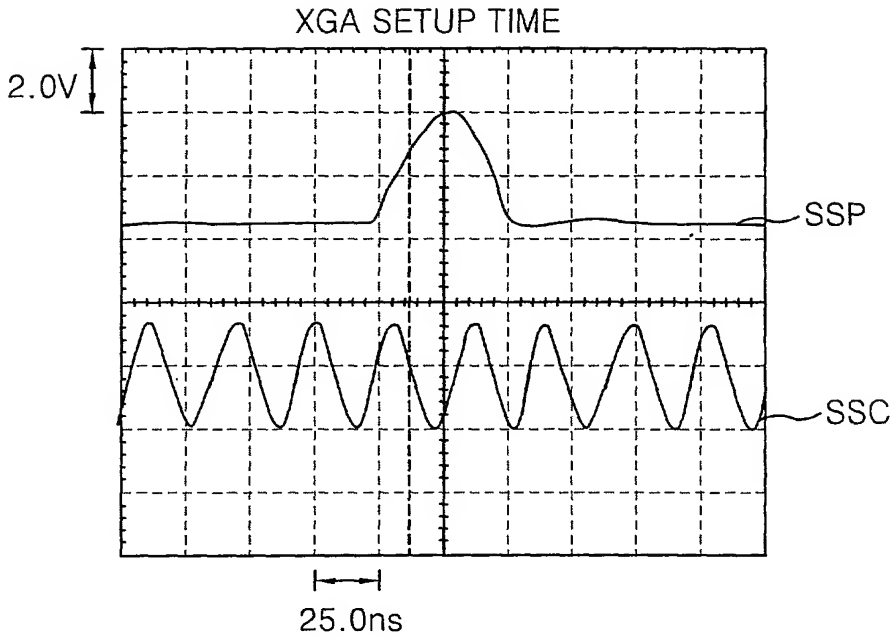

XGA SETUP TIME
2.0V
SSP
SSC
25.0ns

FIG.9B

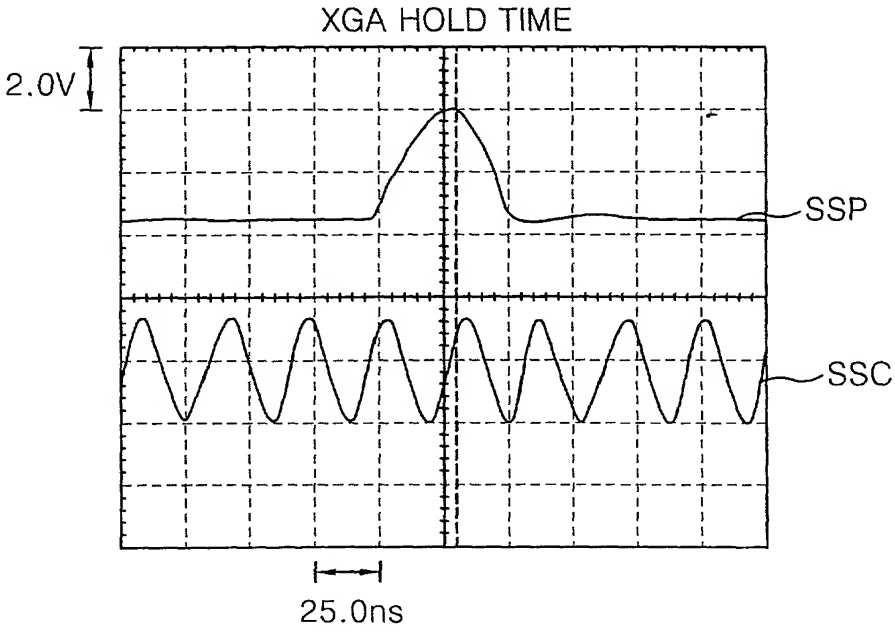

XGA HOLD TIME
2.0V
SSP
SSC
25.0ns

FIG.10A

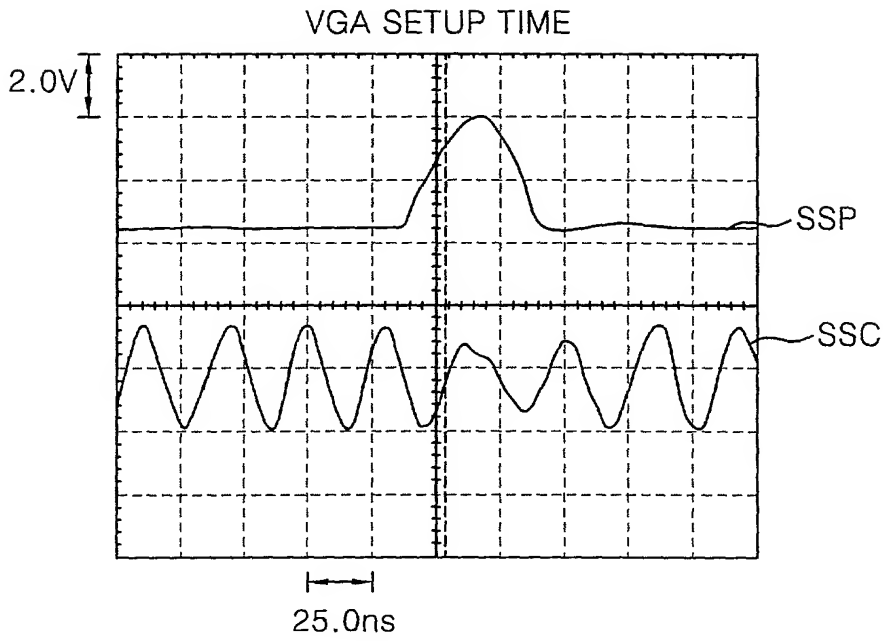


FIG.10B

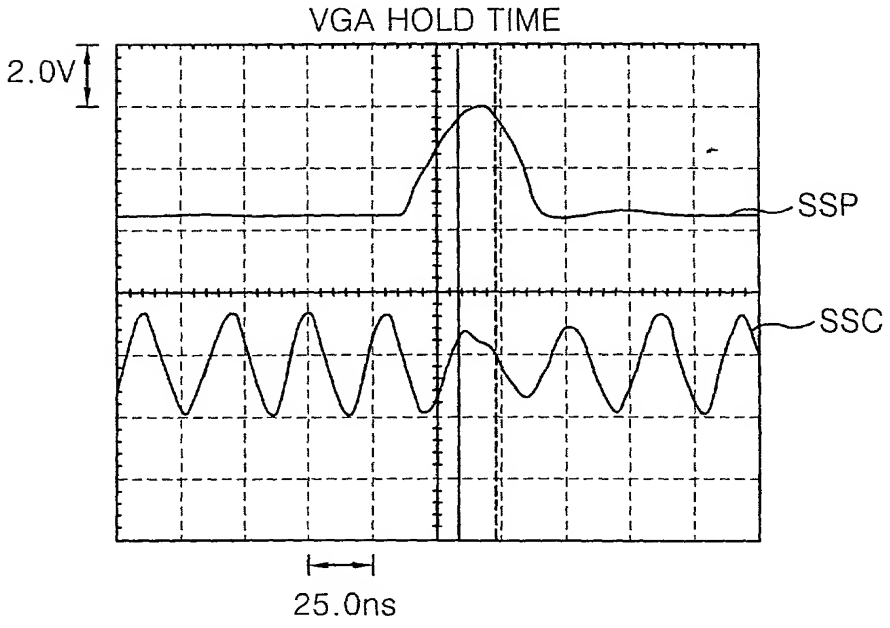


FIG.11A

XGA & VGA SETUP TIME

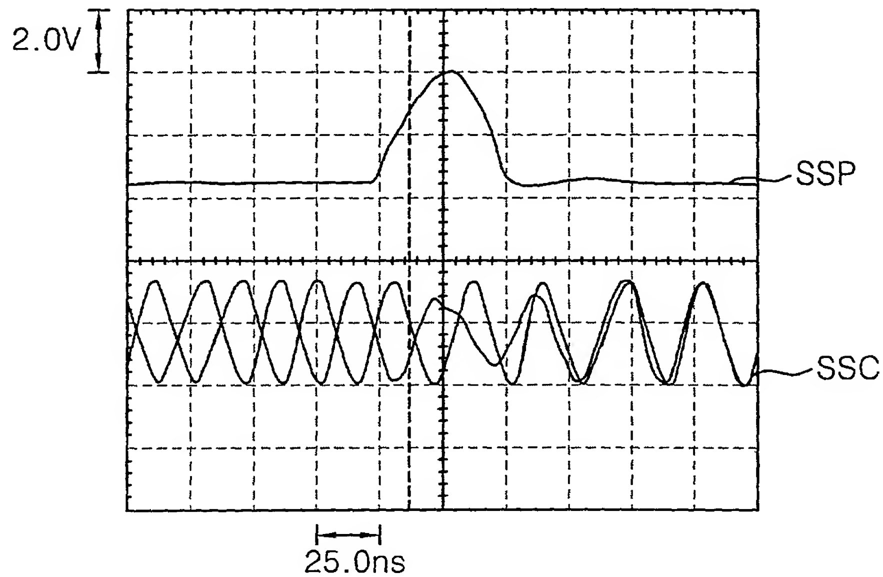


FIG.11B

XGA & VGA HOLD TIME